APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,748	02/16/2000	Raj Kumar Singh	RAL9-99-0181	6579

			EXAMINER
25299	7590	01/13/2004	THANGAVELU, KANDASAMY

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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/505,748	SINGH ET AL.
	Examiner	Art Unit
	Kandasamy Thangavelu	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _16 October 2003_.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-3,6 and 13-17_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-3,6 and 13-17_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _16 February 2000_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1.   This communication is in response to the Applicants' Response mailed on

October 16, 2003. Claims 1, 3 and 6 were amended. Claims 4-5 and 7-12 were

deleted. Claims 13-17 were added. Claims 1-3, 6 and 13-17 of the application are

pending. This office action is made final.

Response to Arguments

2.   Applicants' arguments filed on October 16, 2003 have been fully considered.

The arguments with respect to Claim 1 are moot in view of the new ground(s) of

rejection which are applied against the amended claims. The Applicants' amendments

necessitated the new grounds of rejection.

Drawings

3.   The drawings filed on February 16, 2000 are acceptable subject to correction of

the informalities indicated on the "Notice of Draftperson's Patent Drawing Review,"

PTO-948, sent on December 18, 2002 with paper No. 4.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains.

5.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

6.   Claims 1, 13 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Seawright et al. (SE) (U.S. Parent 5,920,711) in view of **Kim et al. (KI)** (IEEE, August 1999),

Koziotis et al. (KO) (IEEE, October 1999), **Karr et al. (KA)** (U.S. Parent 6,668,297), **Kim et**

al. (KIM) (U.S. Parent 5,978,377), and further in view of **Zwan et al. (ZW)** (U.S. Patent

5,991,270).

6.1   **SE** teaches System for Frame-based protocol, graphical capture, synthesis, analysis and

simulation. Specifically, as per claim 1, **SE** teaches a computer based system employing a

customizable simulation model of an ATM/SONET framer, for system level verification and

performance characterization (Abstract Lines 1-7; CL2, L2-4); comprising:

means for developing an accurate customizable behavioral model that offer sufficient

parameters which can be programmed to represent framers from different vendors (Abstract L4-

10; CL3, L16-20; CL2, L64-66; CL5, L35-46; CL6, L56-58; CL6, L1-2).

SE does not expressly teach a Receiver system and a Transmitter system. **KI** teaches a

Receiver system and a Transmitter system (Page 25, Col 2, Para 2 and Para 3; Fig. 1; Page 26,

Fig 3; Page 26, Col 2, Para 3 and Page 27, Col 1, Para 2; Fig 5), as all communications between

the ATM and the SONET include a Receiver system and a Transmitter system for two-way

communication (Fig. 1; Fig 5; Page 27, Col 2, Para 6 and 7). It would have been obvious to one

of ordinary skill in the art at the time of Applicants' invention to modify the computer based

system of **SE** with the computer based system of **KI** that included a Receiver system and a

Transmitter system, as all communications between the ATM and the SONET include a Receiver

system and a Transmitter system for two-way communication.

SE does not expressly teach that the Receiver system and the Transmitter system are

independently configurable. **KI** teaches that the Receiver system and the Transmitter system are

independently configurable (Page 25, Col 2, Para 2 and Para 3; Fig. 1; Page 26, Fig 3; Page 26,

Col 2, Para 3 and Page 27, Col 1, Para 2; Fig 5), because as per **KIM** it allows implementation of

ATM cell physical layer processing circuits which transmit and receive ATM cells in accordance

with ITU-T and the 16 bit UTOPIA interface of the ATM Forum standard, for the synchronous

optical network (SONET) (CL2, L50-56; CL2, L17-19). It would have been obvious to one of

ordinary skill in the art at the time of Applicants' invention to modify the computer based system

of **SE** with the computer based system of **KI** that included the Receiver system and the

Transmitter system being independently configurable, as it would allow implementation of ATM

cell physical layer processing circuits which transmit and receive ATM cells in accordance with

ITU-T and the 16 bit UTOPIA interface of the ATM Forum standard, for the synchronous optical

network (SONET).

SE does not expressly teach that a Receiver system and a Transmitter system each includes a UTOPIA interface programmable to provide different protocols. **KI** teaches that a Receiver system and a Transmitter system each includes a UTOPIA interface (Page 26, Fig 3; Page 26, Col 2, Para 3 and Page 27, Col 1, Para 2). **ZW** teaches the UTOPIA interface is programmable to provide different protocols, because synchronous optical communication uses OC-1, OC-3, OC-12, OC-48 and other protocols and it is desirable to produce a test device that can fully extract, test and evaluate each of these formats within a single model (CL1, L35-41; Abstract L5-8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer based system of **SE** with the computer based system of **KI** and **ZW** that included that a Receiver system and a Transmitter system each including a UTOPIA interface programmable to provide different protocols, as synchronous optical communication uses OC-1, OC-3, OC-12, OC-48 and other protocols and it would be desirable to produce a test device that can fully extract, test and evaluate each of these formats within a single model.

SE does not expressly teach a first group of buffers operatively coupled to the UTOPIA interface. **KO** teaches a first group of buffers operatively coupled to the UTOPIA interface (Page 1833, Col 2, Para 1; Fig 1), because as per **KI**, the FIFO provides for speed adaptation independent of the external TAM speed (Page 25, Col 2, Para 4 to Page 26, Col 1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer based system of **SE** with the computer based system of **KO** that included a first group of buffers operatively coupled to the UTOPIA interface, because the FIFO would provide for speed adaptation independent of the external TAM speed

SE does not expressly teach SONET Framer Processes including a format translator. **KI** teaches SONET Framer Processes including a format translator (Page 25, Col 2, Para 2 and Para 3; Fig. 1; Page 26, Col 1, Para 2), because as per **KO**, the framer provides for transporting the ATM cells over the SDH/SONET framer at different bit rates (Page 1833, Col 1, Para 1); the SDH framer maps the ATM cells into the payload STS-12c or STS-3c frames in compliance with ITU-T, ATM forum and ANSI specifications; in the receive path, the SDH deframer descrambles the received frame and delivers the ATM cells (Page 1833, Col 1, Para 3 and 4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer based system of **SE** with the computer based system of **KI** that included SONET Framer Processes including a format translator, because the framer would provide for transporting the ATM cells over the SDH/SONET framer at different bit rates; the SDH framer would map the ATM cells into the payload STS-12c or STS-3c frames in compliance with ITU-T, ATM forum and ANSI specifications; in the receive path, the SDH deframer would descrambles the received frame and deliver the ATM cells.

SE does not expressly teach a second group of buffers operatively coupled to the SONET Framer Processes. **KA** teaches a second group of buffers operatively coupled to the SONET Framer Processes (Fig. 1, Blocks 24 and 22; CL5, L5-11), as that allows the POS-PHY packet interface to support transmit and receive transfers at clock rates independent of the line bit rate and support multiple PHY devices (CL5, L5-11). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer based system of **SE** with the computer based system of **KA** that included a second group of buffers operatively coupled to the SONET Framer Processes, as that would allow the POS-PHY packet interface to

support transmit and receive transfers at clock rates independent of the line bit rate and support

multiple PHY devices.

6.2   As per Claim 13, **SE, KI, KO, KA, KIM** and **ZW** teach the system of Claim 1. **SE** does

not expressly teach that the first group of buffers and the Utopia interface are positioned in an

ATM clock domain and the SONET Framer Processes and the second group of buffers are

placed in a SONET clock domain. **KO** teaches that the first group of buffers and the Utopia

interface are positioned in an ATM clock domain and the SONET Framer Processes and the

second group of buffers are placed in a SONET clock domain (Page 1833,Col 1, Para 2; Page

1833,Col 2, Para 3; Page 1834,Col 1, Table 1), because per **KA**, that supports transmit and

receive data transfers at clock rates independent of the line rate (CL5, L5-7).   It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

computer based system of **SE** with the computer based system of **KO** that included the first

group of buffers and the Utopia interface being positioned in an ATM clock domain and the

SONET Framer Processes and the second group of buffers being placed in a SONET clock

domain, as that would support transmit and receive data transfers at clock rates independent of

the line rate.

6.3   As per Claim 3, **SE, KI, KO, KA, KIM** and **ZW** teach the system of Claim 13. **SE** does

not expressly teach that the ATM clock domain and the SONET clock domain operate on

different clock frequencies and represent two distinct clock domains. **KO** teaches that the ATM

clock domain and the SONET clock domain operate on different clock frequencies and represent

two distinct clock domains (Page 1833,Col 1, Para 2; Page 1833,Col 2, Para 3; Page 1834,Col 1,

Table 1), because per **KA**, that supports transmit and receive data transfers at clock rates

independent of the line rate (CL5, L5-7). It would have been obvious to one of ordinary skill in

the art at the time of Applicants' invention to modify the computer based system of **SE** with the

computer based system of **KO** that included the ATM clock domain and the SONET clock

domain operating on different clock frequencies and representing two distinct clock domains, as

that would support transmit and receive data transfers at clock rates independent of the line rate.

6.4   As per claim 17, **SE, KI, KO, KA, KIM** and **ZW** teach the system of Claim 1. **SE** does

not expressly teach that the format translator converts ATM cells to SONET packets and visa

versa. **KI** teaches that the format translator converts ATM cells to SONET packets and visa

versa (Page 25, Col 2, Para 2 and Para 3; Fig. 1; Page 26, Col 1, Para 2), because as per **KO**, the

framer provides for transporting the ATM cells over the SDH/SONET framer at different bit

rates (Page 1833, Col 1, Para 1); the SDH framer maps the ATM cells into the payload STS-12c

or STS-3c frames in compliance with ITU-T, ATM forum and ANSI specifications; in the

receive path, the SDH deframer descrambles the received frame and delivers the ATM cells

(Page 1833, Col 1, Para 3 and 4). It would have been obvious to one of ordinary skill in the art

at the time of Applicants' invention to modify the computer based system of **SE** with the

computer based system of **KI** that included the format translator converting ATM cells to

SONET packets and visa versa, because the framer would provide for transporting the ATM

cells over the SDH/SONET framer at different bit rates; the SDH framer would map the ATM

cells into the payload STS-12c or STS-3c frames in compliance with ITU-T, ATM forum and

ANSI specifications; in the receive path, the SDH deframer would descrambles the received

frame and deliver the ATM cells.

7.   Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Seawright et al.**

(SE) (U.S. Parent 5,920,711) in view of **Kim et al. (KI)** (IEEE, August 1999), **Koziotis et al.**

(KO) (IEEE, October 1999), **Karr et al. (KA)** (U.S. Parent 6,668,297), **Kim et al. (KIM)** (U.S.

Parent 5,978,377), and **Zwan et al. (ZW)** (U.S. Patent 5,991,270), and further in view of

Bagheri et al. (BA) (IEEE, May 1995).

7.1   As per Claim 2, **SE, KI, KO, KA, KIM** and **ZW** teach the system of Claim 1. **SE** does

not expressly teach that the ATM/SONET Framer provides at least one Receiver and at least one

Transmit interfaces to the network at a SONET line rate of 155.52 Mbps(OC-3), 622.08

Mbps(OC-12). **KI** teaches that the ATM/SONET Framer provides at least one Receiver and at

least one Transmit interfaces to the network at a SONET line rate of 155.52 Mbps(OC-3),

622.08 Mbps(OC-12) (Page 25, Col 1, Para 3), because as per **KO**, the framer provides for

transporting the ATM cells over the SDH/SONET framer at different bit rates (Page 1833, Col 1,

Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants'

invention to modify the computer based system of **SE** with the computer based system of **KI** that

included the ATM/SONET Framer providing at least one Receiver and at least one Transmit

interfaces to the network at a SONET line rate of 155.52 Mbps(OC-3), 622.08 Mbps(OC-12), as

the framer would provide for transporting the ATM cells over the SDH/SONET framer at

different bit rates.

SE does not expressly teach that the ATM/SONET Framer provides at least one Receiver

and at least one Transmit interfaces to the network at a SONET line rate of 2488.32

Mbps(OC-48). **BA** teaches that the ATM/SONET Framer provides at least one Receiver and at

least one Transmit interfaces to the network at a SONET line rate of 2488.32 Mbps (OC-48)

(Page 427, Col 1, Para 2), as SONET multiplexers are capable of multiplexing information at

2488.32 Mbps due to recent advances in high speed electronics and light wave systems (Page

427, Col 1, Para 2) and new applications such as high bandwidth video and data services increase

the need for more bandwidth; and such systems result in significant savings in equipment and

operating costs (Page 427, Col 1, Para 2). It would have been obvious to one of ordinary skill in

the art at the time of Applicants' invention to modify the computer based system of **SE** with the

computer based system of **BA** that included the ATM/SONET Framer providing at least one

Receiver and at least one Transmit interfaces to the network at a SONET line rate of 2488.32

Mbps (OC-48), as SONET multiplexers were capable of multiplexing information at 2488.32

Mbps due to advances in high speed electronics and light wave systems and new applications

such as high bandwidth video and data services had increased the need for more bandwidth; and

such systems would result in significant savings in equipment and operating costs.

8.   Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Seawright et al.**

(SE) (U.S. Parent 5,920,711) in view of **Kim et al. (KI)** (IEEE, August 1999), **Koziotis et al.**

(KO) (IEEE, October 1999), **Karr et al. (KA)** (U.S. Parent 6,668,297), **Kim et al. (KIM)** (U.S.

Parent 5,978,377), **Zwan et al. (ZW)** (U.S. Patent 5,991,270), and **Bagheri et al. (BA)** (IEEE,

May 1995), and further in view of **Johnston et al. (JO)** (IEEE, June 1991), **Morrien (MO)**

(U.S. Patent 6,415,325), and **Platt (PL)** (U.S. Patent 5,802,073).

8.1   As per Claim 6, **SE, KI, KO, KA, KIM** and **ZW** teach the system of Claim 1. **SE** does

not expressly teach that the system offers programmability, rich feature set, and two

independently configurable models, one each for the transmit side and the receive side. **KI**

teaches that the system offers programmability, rich feature set, and two independently

configurable models, one each for the transmit side and the receive side (Page 25, Col 2, Para 2

and Para 3; Fig. 1; Page 26, Fig 3; Page 26, Col 2, Para 3 and Page 27, Col 1, Para 2; Fig 5),

because as per **KIM** it allows implementation of ATM cell physical layer processing circuits

which transmit and receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA

interface of the ATM Forum standard, for the synchronous optical network (SONET) (CL2, L50-

56; CL2, L17-19).   It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the computer based system of **SE** with the computer based

system of **KI** that included the system offering programmability, rich feature set, and two

independently configurable models, one each for the transmit side and the receive side, as it

would allow implementation of ATM cell physical layer processing circuits which transmit and

receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA interface of the ATM

Forum standard, for the synchronous optical network (SONET).

SE does not expressly teach that the computer based system offers programmability

features of SONET line rates (OC-Nc: N=1 48; OC-1=51.48 Mbps). **ZW** teaches that the

computer based system offers programmability features of SONET line rates (OC-Nc: N=1 48;

OC-1=51.48 Mbps) (Col 1, Lines 35-41 and Col 6, Lines 30-40), as it is desirable to produce a

test device that can fully test and evaluate each of these formats within a single platform (Col 1,

Lines 35-41).   It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the computer based system of **SE** with the computer based

system of **ZW** that offered programmability features of SONET line rates (OC-Nc: N=1 48;

OC-1=51.48 Mbps), as it would be desirable to produce a test device that could fully test and

evaluate each of these formats within a single platform.

SE does not expressly teach that the computer based system offers programmability

features of percentage of data bytes vs. overhead bytes per row. **BA** teaches that the computer

based system offers programmability features of percentage of data bytes vs. overhead bytes per

row (Page 427, Col 2, Para 2; Fig. 1), as the frame format varies for various STS levels (Page

427, Col 2, Para 2).   It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the computer based system of **SE** with the computer based

system of **BA** that offered programmability features of percentage of data bytes vs. overhead

bytes per row, as the frame format would vary for various STS levels.

SE does not expressly teach that the computer based system offers programmability

features of delays associated with clock domain synchronization. **MO** teaches that the computer

based system offers programmability features of delays associated with clock domain

synchronization (CL1, L51 to CL2, L25), as that allows the nodes to adapt to various measured

clock synchronization delays (CL2, L23-25).   It would have been obvious to one of ordinary

skill in the art at the time of Applicants' invention to modify the computer based system of **SE**

with the computer based system of **MO** that offered programmability features of delays

associated with clock domain synchronization, as that would allow the nodes to adapt to various measured clock synchronization delays.

SE does not expressly teach that the computer based system offers programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update. **KO** teaches that the computer based system offers programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update (Page 1833,Col 1, Para 2; Page 1833, Col 2, Para 1 Page 1834,Col 1, Table 1), because as per **KI**, that allows burst read and write independently of external speed and the FIFO provide for speed adaptation and minimize the latency (Page 25,Col 2, Para4 to Page 26, Col 1, Para 1). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer based system of **SE** with the computer based system of **KO** that offered programmability features of FIFO depth and threshold (in terms of number of cells) and byte or word count threshold within a cell associated with FIFO status update, as that would allow burst read and write independently of external speed and the FIFO would provide for speed adaptation and minimize the latency.

SE does not expressly teach that the computer based system offers programmability features of UTOPIA Level-2/3. **KA** teaches that the computer based system offers programmability features of UTOPIA Level-2/3 (CL1, L19-29), as ATM Forum has proposed these levels and UTOPIA level 2 supports multiple PHY devices and UTOPIA level 3 supports point to point transfer at a maximum throughput of 3.2 Gbps (CL1, L18-29). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

computer based system of **SE** with the computer based system of **KA** that offered

programmability features of UTOPIA Level-2/3, as ATM Forum had proposed these levels and

UTOPIA level 2 would support multiple PHY devices and UTOPIA level 3 would support point

to point transfer at a maximum throughput of 3.2 Gbps.

      SE does not expressly teach that the computer based system offers programmability

features of built-in performance checking. **PL** teaches that the computer based system offers

programmability features of built-in performance checking (Abstract; Fig. 1A, Block 120; CL1,

L65 to CL2, L1), as built-in test logic can be used to achieve a high percentage of fault coverage

for the whole chip (Col 1, Lines 57-59). It would have been obvious to one of ordinary skill in

the art at the time of Applicants' invention to modify the computer based system of **SE** and **KI**

with the computer based system of **PL** that offered programmability features of built-in

performance checking, as built-in test logic can be used to achieve a high percentage of fault

coverage for the whole chip.

9.   Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Seawright
et al. (SE)** (U.S. Parent 5,920,711) in view of **Kim et al. (KI)** (IEEE, August 1999), and

Koziotis et al. (KO) (IEEE, October 1999), and further in view of **Kim et al. (KIM)** (U.S.

Parent 5,978,377)

9.1   As per claim 14, **SE** teaches a computer base method for system level verification and

performance characterization (Abstract Lines 1-7; CL2, L2-4); comprising:

providing a customized behavioral model of an ATM/SONET Framer (Abstract L4-10;

CL3, L16-20; CL2, L64-66; CL5, L35-46; CL6, L56-58; CL6, L1-2).

SE does not expressly teach that the ATM/SONET Framer includes independently

configurable Receiver system and Transmitter system. KI teaches that the ATM/SONET Framer

includes independently configurable Receiver system and Transmitter system (Page 25, Col 2,

Para 2 and Para 3; Fig. 1; Page 26, Fig 3; Page 26, Col 2, Para 3 and Page 27, Col 1, Para 2; Fig

5), because as per KIM it allows implementation of ATM cell physical layer processing circuits

which transmit and receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA

interface of the ATM Forum standard, for the synchronous optical network (SONET) (CL2, L50-

56; CL2, L17-19).   It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the computer based method of SE with the computer based

method of KI that included the ATM/SONET Framer including independently configurable

Receiver system and Transmitter system, as it would allow implementation of ATM cell physical

layer processing circuits which transmit and receive ATM cells in accordance with ITU-T and

the 16 bit UTOPIA interface of the ATM Forum standard, for the synchronous optical network

(SONET).

SE does not expressly teach providing software for coacting with the behavioral model,

the software including sufficient programmable parameters for representing Framers from

different vendors; and activating selected ones of the programmable parameters which cause the

model to behave as a framer from a particular framer manufacturer. KI teaches providing

software for coacting with the behavioral model, the software including sufficient programmable

parameters for representing Framers from different vendors; and activating selected ones of the

programmable parameters which cause the model to behave as a framer from a particular framer

manufacturer (Page 26, Col 1, Para 3 and Page 27, Col 1, Para 5), because as per **KO**, the framer

supports transporting ATM cells over the SDH/SONET network at different bit rates (Page 1833,

Col 1, Para 1) and as per **KIM** it allows implementation of ATM cell physical layer processing

circuits which transmit and receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA

interface of the ATM Forum standard, for the synchronous optical network (SONET) (CL2, L50-

56; CL2, L17-19).   It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to modify the computer based method of **SE** with the computer based

method of **KI** that included providing software for coacting with the behavioral model, the

software including sufficient programmable parameters for representing Framers from different

vendors; and activating selected ones of the programmable parameters which cause the model to

behave as a framer from a particular framer manufacturer, as the framer would support

transporting ATM cells over the SDH/SONET network at different bit rates and it would allow

implementation of ATM cell physical layer processing circuits which transmit and receive ATM

cells in accordance with ITU-T and the 16 bit UTOPIA interface of the ATM Forum standard,

for the synchronous optical network (SONET).

9.2   As per claim 15, **SE, KI, KIM** and **KO** teach the method of Claim 14. **SE** does not

expressly teach providing additional parameters, that causes the model to operate at different line

rates. **KI** teaches providing additional parameters, that causes the model to operate at different

line rates (Page 27, Col 1, Para 5), because as per **KO**, the framer supports transporting ATM

cells over the SDH/SONET network at different bit rates (Page 1833, Col 1, Para 1) and as per

KIM it allows implementation of ATM cell physical layer processing circuits which transmit and receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA interface of the ATM Forum standard, for the synchronous optical network (SONET) (CL2, L50-56; CL2, L17-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer based method of **SE** with the computer based method of **KI** that included providing additional parameters, that causes the model to operate at different line rates, as the framer would support transporting ATM cells over the SDH/SONET network at different bit rates and it would allow implementation of ATM cell physical layer processing circuits which transmit and receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA interface of the ATM Forum standard, for the synchronous optical network (SONET).

9.3   As per claim 16, **SE, KI, KIM** and **KO** teach the method of Claim 15. **SE** does not expressly teach activating selected ones of the additional parameters to cause the model to operate at one of a plurality of line rates. **KI** teaches activating selected ones of the additional parameters to cause the model to operate at one of a plurality of line rates (Page 27, Col 1, Para 5), because as per **KO**, the framer supports transporting ATM cells over the SDH/SONET network at different bit rates (Page 1833, Col 1, Para 1) and as per **KIM** it allows implementation of ATM cell physical layer processing circuits which transmit and receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA interface of the ATM Forum standard, for the synchronous optical network (SONET) (CL2, L50-56; CL2, L17-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the computer based method of **SE** with the computer based method of **KI** that included activating

selected ones of the additional parameters to cause the model to operate at one of a plurality of

line rates, as the framer would support transporting ATM cells over the SDH/SONET network at

different bit rates and it would allow implementation of ATM cell physical layer processing

circuits which transmit and receive ATM cells in accordance with ITU-T and the 16 bit UTOPIA

interface of the ATM Forum standard, for the synchronous optical network (SONET).

Arguments

10.1   As per the applicant's argument that "the claim as amended calls for a receiver system

and a transmitter system; by providing the transmitter and receiver system, applicants provide a

behavioral framer which can be programmed to simulate framers from different framer

manufacturers; neither of the examiners references suggest such a function", the examiner

respectfully disagrees. **KI** teaches a Receiver system and a Transmitter system (Page 25, Col 2,

Para 2 and Para 3; Fig. 1; Page 26, Fig 3; Page 26, Col 2, Para 3 and Page 27, Col 1, Para 2; Fig

5). **SE** teaches a computer based system employing a customizable behavioral model of an

ATM/SONET framer, which can be programmed to represent framers from different framer

manufacturers (Abstract L4-10; CL3, L16-20; CL2, L64-66; CL5, L35-46; CL6, L56-58; CL6,

L1-2).

10.2   As per the applicant's argument that "U.S. Patent 5,920,711 provides a GUI interface and

not a behavioral model for a framer as claimed in the applicants' invention; a GUI interface is

different and inapposite to the teaching to the teaching of a framer as set forth in the amended

claims", the examiner respectfully disagrees. SE (U.S. Patent 5,920,711) states the system

allows the user to generate a High-level description language (HDL) file for the protocol; after

the HDL file is generated, the user can simulate the operation of the HDL (Abstract, L7-10).

Thus this HDL model used for simulation is a high level model and so is behavioral simulation

model. The GUI is used for user interface, for specifying generation of the HDL model for

simulation and for controlling simulation. Applicants' attention is requested to SE, Abstract L4-

10; CL3, L16-20; CL2, L64-66; CL5, L35-46; CL6, L56-58; CL6, L1-2.

Conclusion

ACTION IS FINAL – NECESSIATED BY AMENDMENT

11.   Applicant's amendments necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,
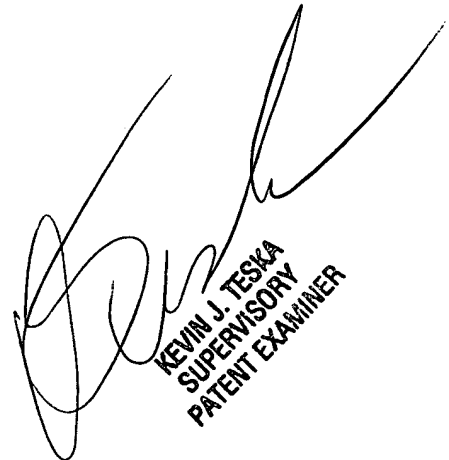
however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

12.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

703-305-0043. The examiner can normally be reached on Monday through Friday from

8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or

proceeding should be directed to the receptionist whose telephone number is 703-305-

9600.

K. Thangavelu
Art Unit 2123
December 31, 2003